Module
8
Testing of Embedded System

Lesson
40
Built-In-Self-Test (BIST) for Embedded Systems

Instructional Objectives

After going through this lesson the student would be able to:

- Explain the meaning of the term 'Built-in Self-Test (BIST)'
- Identify the main components of BIST functionality
- Describe the various methods of test pattern generation for designing embedded systems with BIST
- Define what is a Signature Analysis Register and describe some methods to designing such units
- Explain what is a Built-in Logic Block Observer (BILBO) and describe how to use this block for designing BIST

Built-In-Self-Test (BIST) for Embedded Systems

1.   Introduction

BIST is a design-for-testability technique that places the testing functions physically with the circuit under test (CUT), as illustrated in Figure 40.1 [1]. The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyzer, and a test controller. The test pattern generator generates the test patterns for the CUT. Examples of pattern generators are a ROM with stored patterns, a counter, and a linear feedback shift register (LFSR). A typical response analyzer is a comparator with stored responses or an LFSR used as a signature analyzer. It compares and analyzes the test responses to determine correctness of the CUT. A test control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions can be executed through a test controller circuit.
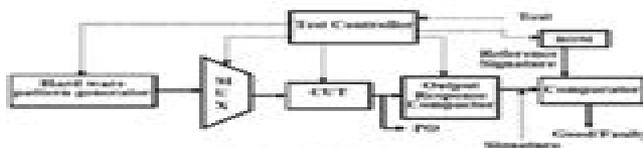

Fig. 40.1 A Typical BIST Architecture

As shown in Figure 40.1, the wires from primary inputs (PIs) to MUX, and wires from circuit output to primary outputs (POs) cannot be tested by BIST. In normal operation, the CUT receives its inputs from other modules and performs the function for which it was designed. During test mode, a test pattern generator circuit applies a sequence of test patterns to the CUT,

and the test responses are evaluated by a output response compactor. In the most common type of BIST, test responses are compacted in output response compactor to form (fault) signatures. The response signatures are compared with reference golden signatures generated or stored on-chip, and the error signal indicates whether chip is good or faulty.

Four primary parameters must be considered in developing a BIST methodology for embedded systems, these correspond with the design parameters for on-line testing techniques discussed in earlier chapter [2].

- *Fault coverage:* This is the fraction of faults of interest that can be exposed by the test patterns produced by pattern generator and detected by output response monitor. In presence of input bit-stream errors there is a chance that the computed signature matches the golden signature, and the circuit is reported as fault free. This undesirable property is called masking or aliasing.
- *Test set size:* This is the number of test patterns produced by the test generator, and is closely linked with fault coverage. Generally, large test sets imply high fault coverage.
- *Hardware overhead:* The extra hardware required for BIST is considered to be overhead. In most embedded systems, high hardware overhead is not acceptable.
- *Performance overhead:* This refers to the impact of BIST hardware on normal circuit performance such as its worst-case (critical) path delays. Overhead of this type is sometimes more important than hardware overhead.

Issues for BIST

- Area Overhead: Additional active area due to test controller, pattern generator, response evaluation and testing of BIST hardware.
- Pin Overhead: At least 1 additional pin is needed to activate BIST operation. Input MUX adds extra pin overheads.
- Performance overhead: Extra path delays are added due to BIST.
- Yield loss: increases due to increased chip area.
- Design effort and time increases due to design BIST.
- The BIST hardware complexity increases when the BIST hardware is made testable.

Benefits of BIST

- It reduces testing and maintenance cost, as it requires simpler and less expensive ATE.
- BIST significantly reduces cost of automatic test pattern generation (ATPG).
- It reduces storage and maintenance of test patterns.
- It can test many units in parallel.
- It takes shorter test application times.
- It can test at functional system speed.

BIST can be used for non-concurrent, on-line testing of the logic and memory parts of a system [2]. It can modify the configured for event-triggered testing, in which case, the BIST control can be tied to the system reset so that testing occurs during system start-up or shutdown. BIST can also be designed for periodic testing with low fault latency. This requires incorporating a testing process into the CUT that guarantees the detection of all target faults within a fixed time.

On-line BIST is usually implemented with the twin goals of complete fault coverage and low fault latency. Hence, the test generation (TG) and response monitor (RM) are generally designed

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